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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,738	10/01/2004	Jen-Ying Chen	FTCP0043USA	5737

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EXAMINER	
DILLON, SAMUEL A	
ART UNIT	**PAPER NUMBER**
2185	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/30/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/711,738	CHEN, JEN-YING	
	Examiner	Art Unit	
	Sam Dillon	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,8 and 10* is/are rejected.

7)☐ Claim(s) *2-7 and 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 October 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. The instant application having Application No. 10/711,738 has a total of 10 claims pending in the application; there are 3 independent claims and 7 dependent claims, all of which are ready for examination by the examiner.

I. INFORMATION CONCERNING OATH/DECLARATION

2. The applicant's oath/declaration has been reviewed by the examiner and is found to conform to the requirements prescribed in 37 C.F.R. ' 1.63.

II. INFORMATION CONCERNING DRAWINGS

3. The applicant's drawings submitted October 1, 2004 are acceptable for examination purposes.

III. REJECTIONS BASED ON PRIOR ART

Claim Rejections - 35 USC ' 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1, 8 and 10** are rejected under 35 U.S.C. 102(b) as being anticipated by Cucchi et al. *(US Patent Number 4,899,352)*.

6. As per **Claim 1**, Cucchi disclose(s) a synchronous memory device with a single port memory unit, the synchronous memory device comprising:

the single port memory unit *(RAM 10, figure 3)* for storing data according to a predetermined clock *(ck channel, figure 3)*;

a configurable write buffer electrically *(FIFO, figure 3)* connected to the single port memory unit for storing data according to the predetermined clock and for transferring its stored data to the single port memory unit according to the predetermined clock *(LFIFO is a dependency of the RAM access control logic, which is a dependency of ck channel, figure 3)*;

a write blocking logic *(write and read counts 14 and 16, figure 3)* electrically connected to the configurable write buffer for estimating a remaining data storage capacity of the configurable write buffer and controlling the configurable write buffer to store data according to the predetermined clock, and for controlling the configurable write buffer to transfer its stored data to the single port memory unit according to a write acknowledge signal *(signal from RAM access control logic 18 to write count 14, figure 3)*; and

an arbiter *(RAM access control logic 18, figure 3)* electrically connected to the write blocking logic and the single port memory unit for generating the write acknowledge signal.

7. As per **Claim 8**, Cucchi disclose(s) a synchronous\asynchronous memory device with a single port memory unit, the synchronous\asynchronous memory device comprising:

the single port memory unit *(RAM 10, figure 3)* for storing data according to a read clock *(ck channel, figure 3)*;

a configurable write buffer *(FIFO 28, figure 3)* electrically connected to the single port memory unit for storing data according to a write clock *(ck source, figure 3)* and for transferring its stored data to the single port memory unit according to the read clock;

a write blocking logic *(write and read counts 14 and 16, figure 3)* electrically connected to the configurable write buffer for estimating a remaining data storage capacity of the configurable write buffer and controlling the configurable write buffer to store data according to the write clock *(data is recorded in according to the ck source clock signal, so can be construed as being a dependency of the loading of the FIFO, figure 3)*, and for controlling the configurable write buffer to transfer its stored data to the single port memory unit according to a write acknowledge signal (*signal from RAM access control logic 18 to write count 14, figure 3)*; and

an arbiter *(RAM access control logic 18, figure 3)* electrically connected to the write blocking logic and the single port memory unit for generating the write acknowledge signal.

8. As per **Claim 10**, disclose(s) a computer system comprising:

a first computer operating on a first clock *(source of 'data in', figure 3)*;

a second computer operating on a second clock different from the first clock *(receiver of 'data out', figure 3)*; and

a memory device *(figure 3)* comprising:

a single port memory unit *(RAM 10, figure 3)* for storing data according to the first clock *(data is loaded into the memory device according to ck source initially, figure 3)*;

a configurable write buffer *(FIFO 28, figure 3)* electrically connected to the single port memory unit for storing data transferred from the first computer according to the first clock *(data is recorded in according to the ck source clock signal, so can be construed as being a dependency of the loading of the FIFO, figure 3)* and for transferring its stored data to the single port memory unit

according to the second clock *(LFIFO is a dependency of the RAM access control logic, which is a dependency of ck channel, figure 3)*;

a write blocking logic *(write and read count's 14 and 16, figure 3)* electrically connected to the configurable write buffer for estimating a remaining data storage capacity of the configurable write buffer and controlling the configurable write buffer to store data transferred from the first computer according to the first clock *(all data is transferred from the first computer according to the first clock, figure 3)*, and for controlling the configurable write buffer to transfer its stored data to the single port memory unit according to a write acknowledge signal *(signal from RAM access control logic 18 to write count 14, figure 3)*; and

an arbiter *(RAM access control logic 18, figure 3)* electrically connected to the write blocking logic and the single port memory unit for generating the write acknowledge signal.

IV. RELEVANT ART CITED BY THE EXAMINER

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Alfke *("Synchronous and Asynchronous FIFO Designs")* discloses an asynchronous elastic buffer.

Drako et al. *(US Patent Number 5,371,877)* disclose using two single port memories to implement an asynchronous elastic buffer. The Examiner notes that the applicant discussed this reference in the specification and is included as a formality.

Nebhrajani ("Asynchronous FIFO Architectures") discloses synchronizing a FIFO to two different clock inputs.

Chou *(US Patent Publication Number 2006/0136620)* discloses a two clocked elastic buffer.

Shyi et al. (*US Patent Number 5426756)* disclose a controller for asynchronous FIFO memory includes with two Gray code counters for determining whether the FIFO is full or empty.

Gerhart (*US Patent Number 5,974,482)* discloses a single port FIFO device having overwrite protection.

Hovagimyan et al. (*US Patent Number 4,056,851)* discloses an elastic buffer, receiving information by a receiving clock, and transmitting an output clock

V. CLOSING COMMENTS

a. STATUS OF CLAIMS IN THE APPLICATION

10. The following is a summary of the treatment and status of all claims in the application as recommended by M.P.E.P. ' 707.07(i):

a(1). SUBJECT MATTER CONSIDERED ALLOWABLE

11. Claims 2-7 and 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. The prior art of record neither anticipates nor renders obvious the below recited combinations:

a. The primary reasons for allowance of Claims 2-7 and 9 in the instant application, but more specifically to Claims 2 and 9, is the combination with the inclusion that:

a write select counter for counting how many data the configurable write buffer has *ever* stored;

a read select counter for counting how many data the configurable write buffer has *ever* transferred;

a demultiplexer for storing data according to the write select counter; and

a multiplexer for transferring data according to the read select counter.

a(4). CLAIMS REJECTED IN THE APPLICATION

12. Per the instant office action, Claims 1, 8 and 10 have received a first action on the merits and are subject of a first action non-final.

b. DIRECTION OF FUTURE CORRESPONDENCES

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Dillon whose telephone number is 571- 272-8010. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sanjiv Shah can be reached on 571-272-4098. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

IMPORTANT NOTE

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Sam Dillon
Examiner
Art Unit 2185

SAD

SANJIV SHAH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100